Weekly status – 3/10/2014

**Task – Defining project scope, short term goals, and long term research goals –**

**Previous week** - Sent out a brief outline of proposal. There are plenty of open ended aspects in the document but the goal is to get clarity on some of the aspects outlined in the proposal as we go forward with the research.

**Progress this week** – Sent out an updated draft proposal to Dr. Tessier. There are plenty of open ended aspects in the document but we are narrowing down and focusing on specifics. Came up with a high level compiler infrastructure that will be developed as part of this research. Got it reviewed by Dr. Tessier. Identified short term goals, specifically developing a switchbox architecture and integrating it to the existing architecture. In addition, also working on custom built core models based on SPREE and trying to see how to integrate them into an existing prototyping framework. Lot of background research involved in this phase.

Blocking issues - None

**Task – Getting started with setting up environment, research tools etc.** –

**Previous week** - Was able to go to the lab and work over the weekend. I now have the software environment and tool setup necessary to do some synthesis work. Have downloaded and started playing around with Altera Quartus tools. Studied some aspects of the DE4 board.

**Progress this week** – Thanks to the help from Meha and Xiaobin, I am now completely setup and able to do my designs, run compilations, simulations and synthesis and do some preliminary analysis on quality of synthesis/P&R results as I am going ahead with the research. I now have moving blocks for all the tools, Quartus based tools for synthesis/p&r, modelsim for simulations, streamit setup for compiler work, router code for starting research on interconnect strategy, SPREE based infrastructure to generate cores and run benchmarks all of which I have been able to successfully do a few iterations from usability perspective. I am currently not focusing on board as I believe that might be less important atleast in initial phases of research

Blocking issues – None

**Task – Study the research on switchbox architecture and see how to integrate it into existing work for supporting course grained reconfigurability**

**Previous week** –Spent time on reading up on switchbox architectures by various groups and how it was done in context of reconfigurable architectures. I did some research on obtaining a template of switchbox Verilog code which we can obtain as starting point.

**Progress this week** – Did a lot of background research reading on design of the switchbox architectures, how to arrange them, and what are the parameters that need to be taken into account to evaluate the power/performance characters especially from standpoint of dynamically reconfigurable architectures. Have started putting together a document outlining some of my research findings, along with what kind of designs I am going to evaluate as part of this goal. I was able to successfully analyze and synthesize an opensource Verilog router code after fixing a few compiler specific issues and failures. However, I could not gather power and performance metrics because p&r failed on this design because the router had more pins than those available in the device. This is not a big deal, because we are only interested in the switchbox part of the router, so I am not going to investigate this failure further. However, this is an important milestone in itself as we now have a working simulateable and synthesizable model out of which we can key off our research designs and do power tradeoffs. In addition, started investigating ow to integrate this switchbox into overall board that Xiaomin is using and am discussing this with him. Have started putting together a document outlining pros/cons of various existing approaches after which I will start adding the approach I will be developing as part of this effort.

Blocking issues – None

**Task – Study the NIOS/Spree architectures**

**Previous week** - Spent some time reading up on NIOS processors that are provided as part of the Altera toolset. Spent time looking into SPREE tools

**Progress this week** – This week, I was able to successfully put together a few example systems with NIOS CPUs and other peripheral devices and able to compile, simulate, synthesize and p&r the designs and see their performance metrics. Was able to successfully generate a few SPREE cores and synthesize/p&r the obtained designs and study their power metrics. Ran some standalone benchmarks on them. We now need to think about starting to put together custom cores onto the reconfigurable architecture environment instead of NIOS based cpu’s. Will discuss in this regard with Dr. Tessier and Xiaomin. Studied how to integrate IPs into stratix environment using the Avalon interconnect (spec here - <http://www.altera.com/literature/manual/mnl_avalon_spec.pdf>) and now have to start thinking about how to integrate the cpu cores that I have been able to synthesize. We will need similar interface in near future for memory integration too (high speed MRAM memory)

Blocking issues – None

**Task – Start looking into StreamIT compiler for studying how to build compiler for course grained reconfigurable architectures**

**Previous week** – downloaded StreamIT compiler. Started playing around with it wrt making the toolset etc. have to start running benchmarks on it and studying the data. Have started reading the research background. Currently reading Dr. Micheal Gordon’s PhD thesis on StreamIT compiler.

**Progress this week** – Continuing to do a lot of background research on StreamIT compiler. Started playing around with running benchmarks on the compiler and studying the results. In addition, I started parsing individual compiler stages as this is essential for us to develop infrastructure for custom compiler development

Blocking issues- None

**Task – Start studying basic approach and algorithms necessary to generate compiler hints for power. In addition start defining steps in the compiler and their requirements to support dynamic course grained reconfigurability**

**Previous week-** None

**Progress this week –** Did a lot of background research on various aspects of this topic. Identified various steps that the compiler will do and presented it as a document to Dr. Tessier. Also, it was decided that I will be using software radio as an initial benchmark. There are several aspects of unresolved issues here as this research will be exploring a lot of things very novel which no one has done before. So there is no good precedence. Algorithms need to be developed on how to characterize power signature analysis from application phases from execution traces and/or dynamic simulation profiles. In addition, these algorithms will need to be refined to include communication aspects. Once these algorithms have been developed and proven by theory/experimentation, we would then need to somehow use this data to generate compiler hints to do dynamic reconfigurability of hardware and perform code generation on the fly so it can be loaded onto a fast MRAM memory. Going forward, I will break this down into sub-topics and start making incremental progress towards defining these aspects more clearly.

**Miscellaneous –** I had a brief exchange of email with Dr. Tessier about lab keys and will be discussing with him the next time I am able to meet him. In addition, also if there is a possibility to get a computer machine allocated to me in the lab to which I can vnc into when working, it might be better. Most of the development I might be doing in initial phase, especially for compiler development, will be in Linux, so a linux box connected to internet might do the trick.